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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,823	03/08/2004	Tzong-Liang Tasi	500-009	2500

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EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,823	TASI ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-8, in the reply filed on May 17, 2005 is acknowledged.

Claim Rejections - 35 USC § 102/35 USC § 103

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as anticipated by Yamasaki et al. '581 or, in the alternative, under 35 U.S.C. 103(a) as obvious over Yamasaki et al. '581 in view of Tomiya et al. '268.

Yamasaki et al. discloses a method for manufacturing a compound semiconductor optoelectronic device comprising steps of forming an

optoelectronic device epitaxial wafer including an Al_2O_3 substrate, an n-GaN layer, an MQW layer, a p-AlGaN layer and a p-GaN layer, forming an insulated isolation material of silicon oxide on the epitaxial wafer, and forming an electrode layer on the epitaxial wafer having the insulated isolation material for completing the optoelectronic device (col. 2, line 64 – col. 3, line 16). Yamasaki et al. does not expressly disclose the epitaxial wafer containing a V-shaped pit due to a threading dislocation, but according to well established physics principles in the area of epitaxial growth of optoelectronic device layers, it is inherent to have a threading dislocation in the epitaxial wafer that creates a V-shaped pit, and thus forming an insulated isolation material of silicon oxide on the epitaxial wafer would inherently fill the V-shaped pit.

Alternatively, assuming arguendo that even if every single device formed according to Yamazaki et al. would not necessarily possess at least one such V-shaped dislocation, it would have nonetheless been obvious for some level of V-shaped pits due to threading dislocations to be typically present on such epitaxial wafers. Tomiya et al. '268 teaches that epitaxial growth techniques of GaN layers result in threading dislocation densities of about $10^6/cm^2$ (col. 1, lines 50-65). The applicant's admitted prior art also states that a dislocation situation in the epitaxy process causes a V-shaped pit to exist in the epitaxial wafer. Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made that the optoelectronic device of Yamasaki et al. would most likely contain V-shaped pits due to threading dislocations as described by Tomiya et al. and/or the applicant's admitted prior art. In such cases in which they are present, the V-shaped pits would have been filled by coating the epitaxial layer with silicon oxide.

Allowable Subject Matter

5. Claims 3-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: a search of the relevant art found references disclosing all elements of claims 1 and 2, but did not find the method of forming an insulated isolation material layer on a V-shaped pit in an epitaxial layer and subsequently removing the isolation material from the surface of the epitaxial layer but leaving the isolation material in the V-shaped pit, as recited in claim 3.

Mishra et al. '144 discloses a method to reduce the dislocation density in group III-nitride films by growing a layer of group III-nitride on a substrate, passivating it with a silicon oxide layer, depositing an interlayer of InGaN, and continuing the group III-nitride layer growth process, however

the silicon oxide is not on the surface of the III-nitride layer stack and the oxide is not removed from any parts of the III-nitride.

Kato et al. '192 and Ota et al. '839 disclose methods of making a group III-nitride device with lower dislocation density by forming a III-nitride film on a substrate, filling dislocations with AlGaN, and continuing to grow the III-nitride film, however an insulating isolation material is not used to passivate dislocations and the AlGaN barrier layer is not removed from portions of the III-nitride film.

Morita et al. '648 and Lee at el. '389 disclose methods to produce a crystalline film with low dislocation density formed by growing a monocrystalline layer on a substrate, etching the material to create pits along dislocations, filling the pits by coating the monocrystalline layer with silicon oxide or InGaN, and continuing to grow the monocrystalline layer. In both references, the pits are exacerbated by etching, and the silicon oxide barrier layer is not removed from any portion of the monocrystalline layer.

Watanabe et al. '846 discloses a method of manufacturing a nitride semiconductor device wherein a GaN film is formed on a substrate, and a second GaN layer is deposited on top of the first to fill in dislocations and prevent their further propagation. Hahn et al. '226 discloses a method of fabricating an LED comprising GaN layers, wherein the GaN layers have controlled thickness to control the development and propagation of

dislocations. Neither reference discloses the use of an insulating barrier layer to passivate dislocations.

Nagai et al. '806 and Yang '823 disclose methods of manufacturing an LED comprising group III-V layers, wherein the final surface layer is passivated by a silicon oxide layer. Neither reference discloses removing portions of the silicon oxide from the surface and leaving portions in dislocation pits.

Nicolay et al. '207 discloses a method for fabricating isolated regions in a semiconductor device wherein V-shaped grooves are etched into the semiconductor surface, a field oxide is formed to fill the grooves, and the oxide is etched back to the semiconductor surface. This method is related to field oxide isolation and not to the passivation of group III-nitride dislocation pits.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sjf
8/10/05

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER